



Still alive!

It's not yet time to write the asic's obituary. By **Paul Dempsey**.

The topic at this year's Globalpress Electronics Summit was provocative: 'Can anything save asics?' and the question drew lively responses from a broad based panel.

Our *dramatis personae*. Three came from asic design. Elie Massabki, vp of marketing at ChipX, Naveed Sherwani, chairman and ceo of Open Silicon, and Hugh Durdan, vp of marketing for eSilicon. They represent a newer breed of 'fabless asic' specialist, although work with both oems and silicon vendors.

From over the fence came Dennis Kish, vp of marketing for fpga specialist Actel, and Steve Carlson, vp of marketing for Cadence Design Systems.

Whilst there was consensus that the business has changed – and will continue to do so – Kish disputed the notion that asics are at death's door.

"According to Gartner, asics were a \$23billion market last year and, from 2002 to 2010, will grow a little faster than the overall semiconductor market," he noted. "That's got me scratching my head. Why are we debating whether or not asics can survive when the numbers are going up and to the right?"

Rather, it seems the traditional asic model is in terminal trouble. "Historically, an asic was a custom chip done by a sys-

tem oem to add value and differentiation. There is evidence this activity is in decline – look at design starts," said Durdan.

"The dynamic is that system oems have had a hard time justifying the expense and risk of developing custom solutions. Instead, they rely increasingly on standard products, shifting risk and development costs to semiconductor companies."

Kish took a similar tack. "An asic these days is a thinly veiled assp. It probably started life as an assp platform, like [Texas Instruments'] OMAP, was adapted for a specific technology – say mobile phones – based on technology where the vendor has a leadership position – say dsp.

"Chip vendors began to develop deep expertise in particular applications and their aspps became demo chips. Low volume users adopt them directly; high volume users go back and negotiate to get

asics adapted to their value propositions."

Sherwani acknowledged this trend has impinged upon the asic market. "One of our customer bases is those building aspps for spaces where, initially, there is little volume. A bunch of start ups – at any time, there may be 200 – innovate and build 'introduction to aspp market' chips. For three or four years, they do business, then someone like Marvell or Broadcom enters the space and kills their products," he said. "Eventually, in any market that becomes large and stable, the large players arrive and eat everybody else's lunch."

But that does not mean asic companies can't see opportunities to make money.

Acknowledging the traditional model is 'dying a slow and painful death', Carlson added: "We've given birth to new models and it's interesting to watch what's being experimented with. We're going through a



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Massabki (right): "We don't have any favourites – we have structured asics, we have embedded arrays, we have standard cell and we love 'em all."





transition and there's a lot of confusion. It's a result of trying to understand the trade offs between those models."

He added that market complexity was not just about competition from fpgas and asps, but also about complications from software programmability and 'a technology foundation in constant flux'.

In short, the asic debate is a subset of the broader topic of design management and design efficiency.

Sherwani cited two other mainstays for his company. "One is where a typical semiconductor company is not interested – the volume is not there and never will be because it is a niche," he said. "Another is for fleeting markets. With long design cycles, big players cannot wake up in time. A small company can get in, get \$40 or 50million of business and get out. It's less about integration, more about time to market."

From an architectural perspective, Massabki emphasised a horses for courses approach, with particular reference to structured asic – a once 'hot' market which cooled after withdrawals by NEC and LSI.

"We don't have any favourites – we have structured asics, we have embedded arrays, we have standard cell and we love 'em all," he said. "It's about the fit. Structured asics work where a customer wants so many gates, so much memory and cer-

tain IP. If it's available in a structured asic, it's the best fit because NREs are very low and time to market is faster than for other methodologies. The drawback is that if the fit isn't there, you need the other solutions. It all depends on the customer's priorities and requirements."

Massabki described another approach that he sees becoming increasingly popular. "Sometimes, more integration is not the right solution. Instead, you can have a smart architecture, with a fixed functionality that doesn't change and something next to it that varies. We label this a 'side chip architecture' and it doesn't need to be programmable," he said. "You have a main asic – 10 or 20m gates – and a small chip with maybe 100,000 gates. You can respin that quickly, use it for regionalisation and customise it. Now, not everyone has to pay to build one fully integrated chip with all the functionality."

This parallels how fpgas address the market. Kish said: "A chip that is 95% fixed with some programmability is the essence of what will succeed in the long term."

Multiple models, then, but as they chum through Carlson's 'transition phase', one other question arises: how much of the perceived 'problem' is attributable to asic specialists?

"Why have asics survived? They didn't


deserve to. Ridiculous cost, extremely unpredictable, extremely unreliable. Traditional asic vendors did everything in their power to kill the market," said Sherwani.

"They have survived because they are needed. At the end of the day, hardware is what differentiates one company from another. You can never do in software what you can do in hardware. I've been a designer all my life and you can do magic with transistors."

Open Silicon and eSilicon have responded to perceived market inefficiency with disciplined, universal design flows used across all projects. The results?

"In eSilicon's history – we've done hundreds of tape outs – there is only one instance where we introduced a problem into a customer's design," said Durdan.

Sherwani added: "90% of the delays in our chips are caused by customers; we cause 10%. We are 88% predictable and 94% reliable. But we only solve 10% of the problem. This tells you that whatever customers are doing to write and verify their RTL, either they're not disciplined or the process is so artistic that it may not be open to discipline."

The message here is that, whilst the asic business is cleaning up its act, problems persist elsewhere in the custom chain. And this opens up the custom debate to issues beyond asic's longevity. 

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